I CLAIM:

1. An integrated circuit chip mounted on a leadframe, comprising:

a network of power distribution lines deposited on the surface of said chip, located directly over active components of said circuit; and

said lines conductively and vertically connected to selected active components below said lines, and also by conductors connected to segments of said leadframe,

thereby saving silicon real estate consumed by circuit power distribution lines and conductor pads, gaining circuit design flexibility and assembly manufacturability, and reducing input/output numbers of said segments.

2. A semiconductor device having an additional conductor network on the chip surface, wherein the power distribution of the integrated circuit is combined with the power distribution of the leadframe, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer, and a plurality of windows to expose circuit contact pads;

electrically conductive films deposited on said overcoat and patterned into a network of lines

substantially vertically over said active components, said films in contact with said vias and having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

said network patterned to distribute power current and ground potential;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said chip contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

3. The device according to Claim 2 wherein said chip is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic device fabrication.

4. The device according to Claim 2 wherein said circuit comprises a plurality of active and passive electronic components arranged horizontally and vertically.

5. The device according to Claim 2 wherein said integrated circuit comprises multi-layer metallization, at least one of said layers made of pure or alloyed copper, aluminum, nickel, or refractory metals.

6. The device according to Claim 2 wherein said overcoat comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon

alloys, polyimide, and sandwiched films thereof.

7. The device according to Claim 2 wherein said leadframe is pre-fabricated from a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.

8. The device according to Claim 2 further comprising an encapsulation enclosing said chip, chip mount pad, electrical conductors, and at least portions of said leadframe segments.

9. The device according to Claim 8 wherein said encapsulation comprises a polymer compound fabricated on a transfer molding process.

10. The device according to Claim 8 wherein leadframe segment portions not included in said encapsulation are shaped as leads or pins, solderable to outside parts.

11. The device according to Claim 2 wherein said lines and contact pads are attached to outside parts by solder balls.

12. The device according to Claim 2 wherein said metallurgical attachment comprises wire ball and stitch bonding, ribbon bonding, and soldering.

13. The device according to Claim 2 wherein said electrically conductive films comprise at least one stress-absorbing metal layer selected from a group consisting of copper, nickel, aluminum, tungsten, titanium, molybdenum, chromium, and alloys thereof.

14. The device according to Claim 2 wherein said outermost metal layer is selected from a group consisting of pure or alloyed gold, palladium, silver, platinum, and aluminum.

15. The device according to Claim 2 wherein said conductors are bonding wires, bonding ribbons, or solder balls.

16. The device according to Claim 15 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

17. The device according to Claim 15 wherein said solder ball is selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

18. The device according to Claim 2 wherein said network of lines is electrically further connected to selected segments suitable for outside electrical contact.

19. The device according to Claim 2 wherein said network of lines, together with said metal-filled vias, provides the power distribution function between said active circuit components.

20. A method for fabricating a semiconductor device including a semiconductor chip having first and second surfaces, comprising the steps of:

forming an integrated circuit on said first chip surface, said circuit including active components, at least one metal layer, and a mechanically strong, electrically insulating protective overcoat;

forming a plurality of vias through said overcoat to access said at least one metal layer;

filling said vias by depositing a stack of metal films on said overcoat, said stack having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

patterning said films into a network of lines such that said lines are located substantially

vertical over said active components and are suitable for power current distribution;

forming a plurality of windows in said overcoat to expose circuit contact pads;

providing a pre-fabricated leadframe comprising a chip mount pad, a first plurality of segments suitable for electrical signals, and a second plurality of segments suitable for electrical power and ground;

attaching said chip to said chip mount pad;

attaching electrical conductors to said circuit contact pads and said first plurality of segments; and

attaching electrical conductors to said network of lines and said second plurality of segments.

21. The method according to Claim 20 wherein said steps of attaching electrical conductors to said contact pads and said network of lines comprise the step of either bonding wires or ribbons to said contact pads and network of lines, or reflowing solder balls to said contact pads and network of lines.

22. The method according to Claim 20 further comprising the step of encapsulating said chip, chip mount pad, electrical conductors and at least a portion of said leadframe segments in a package.

23. The method according to Claim 20 further comprising the step of attaching said circuit contact pads and said network of lines to outside parts by solder balls.